Access DB# 67465

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: P. Laufer Examiner# : _____ Date: 5/28/02

Art Unit: 2100 Phone Number: 306-4160 Serial Number: _____

Mail Box and Bldg/Room Location: _____ Results Format Preferred (circle): Paper Disk E-mail

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

_____

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

5,961,621

****

STAFF USE ONLY

Searcher: S Green

Searcher Phone: 6-4767

Searcher Location: 4B40

Date Searcher Picked Up: 5/28/02

Date Completed: 5/28/02

Searcher Prep & Review Time: 5

Clerical Prep Time: _____

Online Time: 15

Type of search

NA Sequence (#) _____

AA Sequence (#) _____

Structure (#) _____

Bibliographic _____

Litigation ✓

Full Text _____

Patent Family _____

Other _____

Vendors and cost where applicable

STN _____

Dialog _____

Questel/Orbit 15.79

Dr. Link _____

Lexis/Nexis _____

Sequence System _____

WWW/Internet _____

Other (specify) _____

Green, Shirelle

From: Laufer, Pinchus
Sent: Monday, May 27, 2002 11:28 AM
To: Green, Shirelle
Subject: litigation searches

Please generate searches for:

(1) US Patent No 5,961,621 Re. S.N. 09/972,704 Inventors: William S. Wu et al.
Owner of Record: INTEL (Appeared in OG 5/07/02)

(2) US Patent No 6,021,265 Re. S.N. 10/066,475 Inventors: Edward Colles Nevill
Owner of Record: ARM Limited, Cambridge, England (Appeared in OG 5/14/02)

(3) US Patent No 5,961,614 Re. S.N. 09/972,847 Inventors: Kevin Christiansen
Owner of Record: APPLE Computer (Appeared in OG 5/21/02)

(43) US Patent No 5,970,255 Re. S.N. 10/084,757 Inventors: Nghia Tran et al.
Owner of Record: ALTERA Corporation (Appeared in OG 5/21/02)

Thank You,

Pinchus

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(703) 306-4160
plaufer@uspto.gov

05-28-02 A10:38 IN

1 of 1 DOCUMENT

5,961,621

GET 1st DRAWING SHEET OF 4

Oct. 5, 1999

Mechanism for efficiently processing deferred order-dependent memory access transactions in a pipelined system

REISSUE:
Reissue Application filed Oct. 4, 2001 (O.G. May 7, 2002) Ex. Gp.: 2185; Re. S.N. 09/972,704

INVENTOR:
Wu, William S., Cupertino, California
MacWilliams, Peter D., Aloha, Oregon
Pawlowski, Stephen, Beaverton, Oregon
Jayakumar, Muthurajan, Sunnyvale, California

ASSIGNEE-AT-ISSUE:
Intel Corporation, Santa Clara, California (02)

APPL-NO:
827,540

FILED:
Mar. 28, 1997

INT-CL:
[6] G06F 13#00

US-CL:
710#107; 710#100; 711#140; 711#146; 711#169

SEARCH-FLD:
395#292, 282, 309, 392, 395, 380, 381, 382; 711#140, 146, 141, 118, 169, 168

PRIM-EXMR:
Chan, Eddie P.

ASST-EXMR:
McLean, Kimberly N.

LEGAL-REP:
Blakely, Sokoloff, Taylor & Zafman LLP

No Documents Found

No documents were found for your search (**5961621 or 5,961,621**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: JNLS

No Documents Found

No documents were found for your search (**5961621 or 5,961,621**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: CASES

?us5961621/pn

** SS 1: Results 1

Search statement 2

?prt full nonstop legalall

1/1 PLUSPAT - (C) QUESTEL-ORBIT- image
PN - US5961621 A 19991005 [US5961621]
TI - (A) Mechanism for efficiently processing deferred order-dependent memory access transactions in a pipelined system
PA - (A) INTEL CORP (US)
IN - (A) MACWILLIAMS PETER D (US); PAWLOWSKI STEPHEN (US); WU WILLIAM S (US); JAYAKUMAR MUTHURAJAN (US)
AP - US82754097 19970328 [1997US-0827540]
PR - US82754097 19970328 [1997US-0827540]
IC - (A) G06F-013/00
EC - G06F-013/16
PCL - ORIGINAL (O) : 710107000; CROSS-REFERENCE (X) : 710100000 711140000 711146000 711169000
DT - Basic
CT - US5682516; US5761444; US5774700; US5778438
- Pentium Pro Family Developer's Manual Volume: Specifications, Chapters 4-5, Dec. 1996.
STG - (A) United States patent
AB - A bus agent defers an ordered transaction if the transaction cannot be completed in order. When an ordered transaction is deferred, its visibility for the next ordered transaction is asserted if it can guarantee a sequential order of the ordered transaction and the next ordered transaction. This visibility indication allows the bus agent to proceed with the next ordered transaction without waiting for the completion status of the deferred transaction. The visibility indication provides fast processing of ordered transactions.

1/1 LGST - (C) LEGSTAT
PN - US 5961621 [US5961621]
AP - US 827540/97 19970328 [1997US-0827540]
DT - US-P
ACT - 19970328 US/AE-A
APPLICATION DATA (PATENT)
{US 827540/97 19970328 [1997US-0827540]}
- 19971027 US/AS02
ASSIGNMENT OF ASSIGNOR'S INTEREST
INTEL CORPORATION 2200 MISSION COLLEGE BOULEVARD SANTA CLARA, CALIFORNIA 95052 * WU, WILLIAM S. : 19970326; MACWILLIAMS, PETER D. : 19971021; PAWLOWSKI, STEPHEN : 19971021; JAYAKUMAR, MUTHURA : 19970327
- 19991005 US/A
PATENT
- 20020507 US/RF
REISSUE APPLICATION FILED
20011004
UP - 2002-20

1/1 CRXX - (C) CLAIMS/RRX
PN - 5,961,621 D 19991005 [US5961621]
PA - Intel Corp
ACT - 20011004 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20020507
REISSUE REQUEST NUMBER: 09/972704

EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2185

Reissue Patent Number:

1/1 PAST - (C) Thomson Derwent
AN - 200219-001724
PN - 5961621 A [US5961621]
OG - 2002-05-07
ACT - REISSUE APPLICATION FILED

fam us5961621/pn

1 Patent Groups
** SS 1: Results 1

Search statement 2

?famstate nonstop

1/1 INPADOC - (C) INPADOC
PN - US 5961621 A 19991005 [US5961621]
TI - MECHANISM FOR EFFICIENTLY PROCESSING DEFERRED ORDER-DEPENDENT MEMORY ACCESS TRANSACTIONS IN A PIPELINED SYSTEM
IN - WU WILLIAM S [US]; MACWILLIAMS PETER D [US]; PAWLOWSKI STEPHEN [US]; JAYAKUMAR MUTHURAJAN [US]
PA - INTEL CORP [US]
AP - US 827540/97-A 19970328 [1997US-0827540]
PR - US 827540/97-A 19970328 [1997US-0827540]
IC - G06F-013/00

1/1 LEGALI - (C) LEGSTAT
PN - US 5961621 [US5961621]
AP - US 827540/97 19970328 [1997US-0827540]
DT - US-P
ACTE- 19970328 US/AE-A
APPLICATION DATA (PATENT)
{US 827540/97 19970328 [1997US-0827540]}
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INTEL CORPORATION 2200 MISSION COLLEGE BOULEVARD SANTA CLARA, CALIFORNIA 95052 * WU, WILLIAM S. : 19970326; MACWILLIAMS, PETER D. : 19971021; PAWLOWSKI, STEPHEN : 19971021; JAYAKUMAR, MUTHURA : 19970327
- 19991005 US/A
PATENT
- 20020507 US/RF
REISSUE APPLICATION FILED
20011004
UP - 2002-20